IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant : Shunpei Yamazaki et al. Art Unit : 2823
Serial No. : 09/635,832 Examiner : Fernando Toledo
Filed : August 9, 2000
Title : SEMICONDUCTOR DEVICE HAVING SOI STRUCTURE AND MANUFACTURING METHOD THEREFOR

Do not enter 4/24/06

MAIL STOP AF
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

REQUEST FOR RECONSIDERATION IN REPLY TO ACTION OF FEBRUARY 6, 2006

Applicant submits the following remarks in response to the office action of February 6, 2006.

Claims 18-37, 39-56, 58-64, 66-72, 74-80, 82-88, 90-96, 98-104, 106-130 and 133-142 are pending, with claims 18, 19, 58-64 and 135 being independent. Claims 18-37, 39-56, 59, 60, 63, 64, 67, 68, 71, 72, 75, 76, 79, 80, 83, 84, 87, 88, 91, 92, 95, 96, 99, 100, 103, 104, 107, 108, 111, 112, 115, 116, 119, 120, 123, 124, 127 and 128 have been withdrawn from consideration, leaving independent claims 58, 61, 62 and 135 under consideration along with their dependent claims 66, 69, 70, 74, 77, 78, 82, 85, 86, 90, 93, 94, 98, 101, 102, 106, 109, 110, 113, 114, 117, 118, 121, 122, 125, 126, 129, 130, 133, 134 and 136-142.

Applicant acknowledges with appreciation the Examiner's allowance of claims 58, 62, 66, 70, 74, 78, 82, 86, 90, 94, 98, 102, 106, 110, 114, 118, 122, 126 and 130, and the Examiner's indication that claims 121, 125, 140 and 141 are directed to allowable subject matter.

Claims 61, 85, 93 and 135 have been rejected as being anticipated by Ozaki (U.S. Patent No. 5,028,976). Applicant requests reconsideration and withdrawal of this rejection because Ozaki does not describe or suggest an arrangement in which the first transistor is an **n-channel transistor** and includes a first impurity element that belongs to group 13 (i.e., a **p-type impurity element**) in its channel forming region, and the second transistor is a **p-channel transistor** and includes a second impurity element that belongs to group 15 (i.e., an **n-type impurity element**) in its channel forming region, as recited in claim 61, or an arrangement in which the first transistor is an **p-channel transistor** and includes a first impurity element that belongs to group